PRECISION ELECTRONIC DIGITAL CLOCK USES IC'S

by Jack Irwin and Robert Jensen

SUMMARY

A precision digital clock with a 1-Mc crystal-controlled oscillator as the basic timing source and an accuracy of one part in one-hundred million has been built. This clock uses 72 Fairchild integrated circuits and has a built-in preset capability to count seconds, minutes, and hours.

INTRODUCTION

A 1-Mc crystal-controlled oscillator serves as the basic timing source for a precision digital clock utilizing Fairchild integrated circuits. At this relatively high frequency, crystals achieve a greater degree of stability and accuracy than at lower frequencies. The oscillator output is coupled directly to the first stage of a series of six decade counters. These counters divide the 1-Mc timing signal by one million. The resulting 1-cps signal is the basic reference for all further timing in the clock.

DESCRIPTION OF DIGITAL CLOCK

The system is iterative by nature. A general block diagram of the clock is shown in Fig. 2. Notice the iterative nature of much of the circuitry; i.e., the logic circuits for seconds, minutes and hours are all alike, as are the circuits for tens of seconds and tens of minutes. As it results in simpler circuitry, the clock follows the traditional United States method of keeping time and recycles to 01:00:00 o'clock at 12:59:59 o'clock plus one second. The Continental method, going from 0 hours to 24 hours, would require additional circuits in the last two stages.

*Reprinted with permission of Electronic Design 26, November 22, 1966.

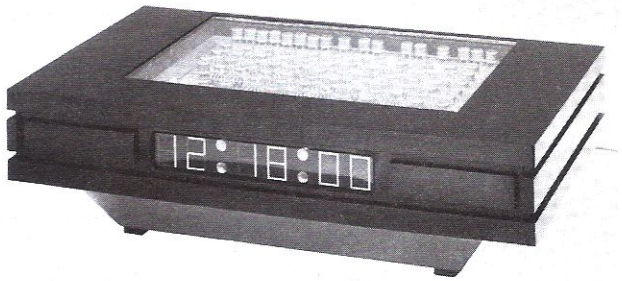


Fig. 1. Digital clock built with 90 integrated circuits.

Using an integrated decade counter drastically reduces the actual number of elements needed for implementation: Only six packages are needed to form the basic frequency divider network. The particular counter used (Fairchild 9958) is functionally shown in Fig. 3a; the relative position of the wave forms at the output appears in Fig. 3b. A positive transition occurs at output D as the count goes from nine to zero. Since this is the only positive transition at this terminal, this output can be coupled directly into the input of the next stage.

Because this counter provides a BCD output, it is also used as the unit's counter circuit for seconds, minutes and hours.

To count tens of seconds and tens of minutes, a modulo-6 counter is required. There is a wide choice of possible circuitry, so that selection becomes highly subjective. Because of its low power-dissipation rating, high fan-out, and ready availability, Fairchild 9913 flip-flop was used as the basic element for the modulo-6 counter. This counter,

COPYRIGHT, FAIRCHILD SEMICONDUCTOR, 1967 • PRINTED IN U.S.A. 2320-131-17 35M

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.

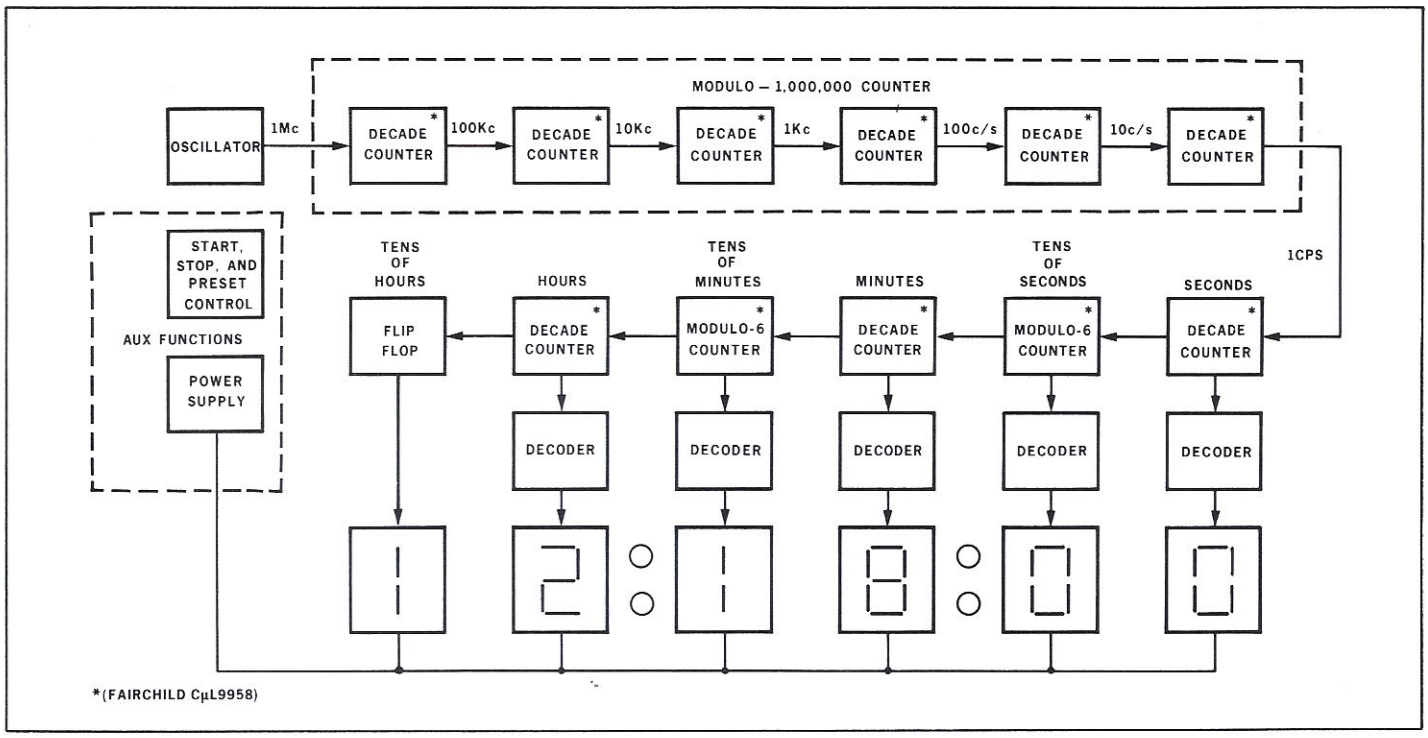


Fig. 2. The four fundamental units of the clock.

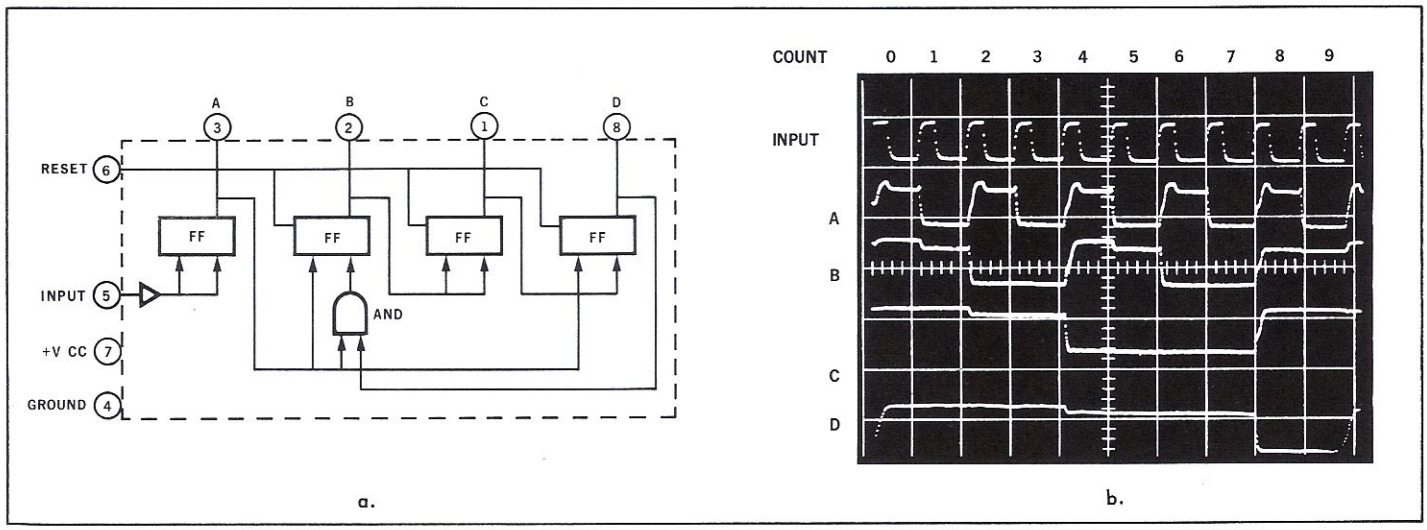
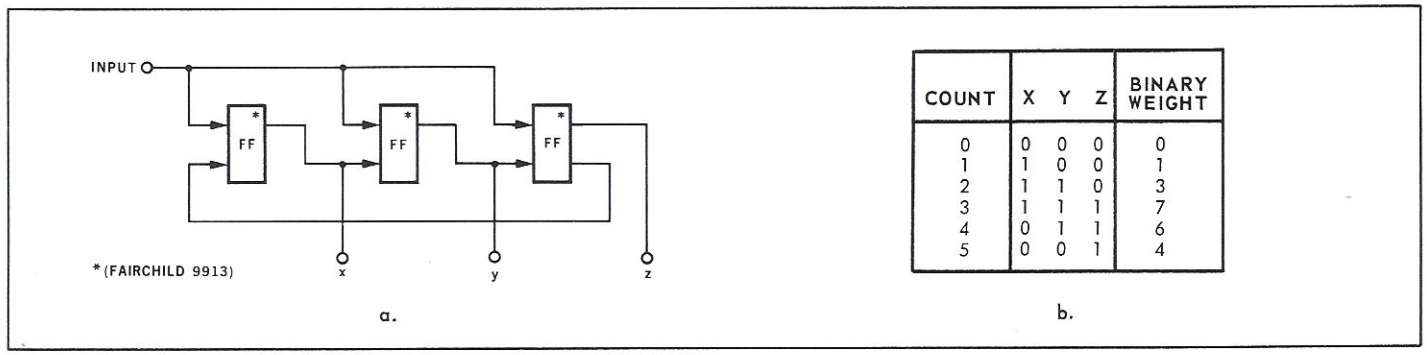


Fig. 3. Complete integrated decade counter.



COUNT	X	Y	Z	BINARY WEIGHT
0	0	0	0	0
1	1	0	0	1
2	1	1	0	3
3	1	1	1	7
4	0	1	1	6
5	0	0	1	4

Fig. 4. Modulo-6 counter uses three flip-flops.

functionally shown in Fig. 4a, is a shift-mode counter, known also as a "walking clock" or "twisted-ring counter." The timing chart for this counter is given in Fig. 4b; on the sixth count, all outputs return to their initial state.

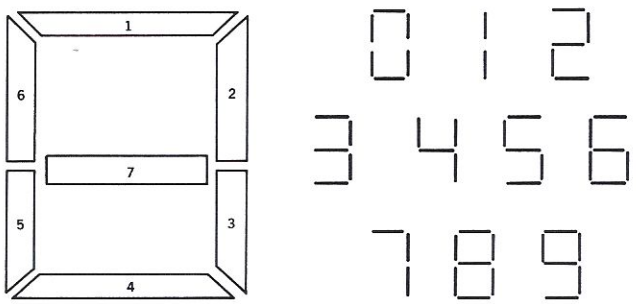


Fig. 5. Incandescent display has seven segments.

For the displays, six incandescent indicators were selected. Use of an incandescent display, as opposed to a gas-tube display, simplified the power supply design. This includes a direct connection to a set of rechargeable batteries so that stand-by power is available. The segmented indicator layout is illustrated in Fig. 5, along with the segmented display of the numerals 0 through 9.

OPERATION

The states of the unit's counters are decoded as the counters progress through their cycles so that the appropriate indicator segments may be lighted extinguished. Since more segments are generally ON than OFF, the better method of indication is to extinguish superfluous lights rather than to illuminate needed lights. Note also that the numbers 6 could be represented with or without segment 1, and likewise the numbers 9 with or without segment 4; inclusion of these bars, however, lessens the amount of extinguishing that has to be done.

A set of logic equations, as a function of each segment, can be written for the numbers that have to be displayed. These take the form:

$$\overline{f}_1 = (1+4+10+11+12+13+14+15),$$
$$\overline{f}_2 = (5+6+10+11+12+13+14+15),$$
$$\overline{f}_3 = (2+10+11+12+13+14+15),$$
$$\overline{f}_4 = (1+4+7+10+11+12+13+14+15),$$
$$\overline{f}_5 = (1+3+4+5+7+9+10+11+12+13+14+15),$$
$$\overline{f}_6 = (1+2+3+7+10+11+12+13+14+15),$$
$$\overline{f}_7 = (0+1+7+10+12+13+14+15).$$

The symbol for negation above (—), means extinction as opposed to ignition. Because all four binary varables are being dealt with, there is a possibility of sixteen states (0-15); but as the decade counter completes its cycle on the tenth count, states 10-15 will never occur and can thus be included

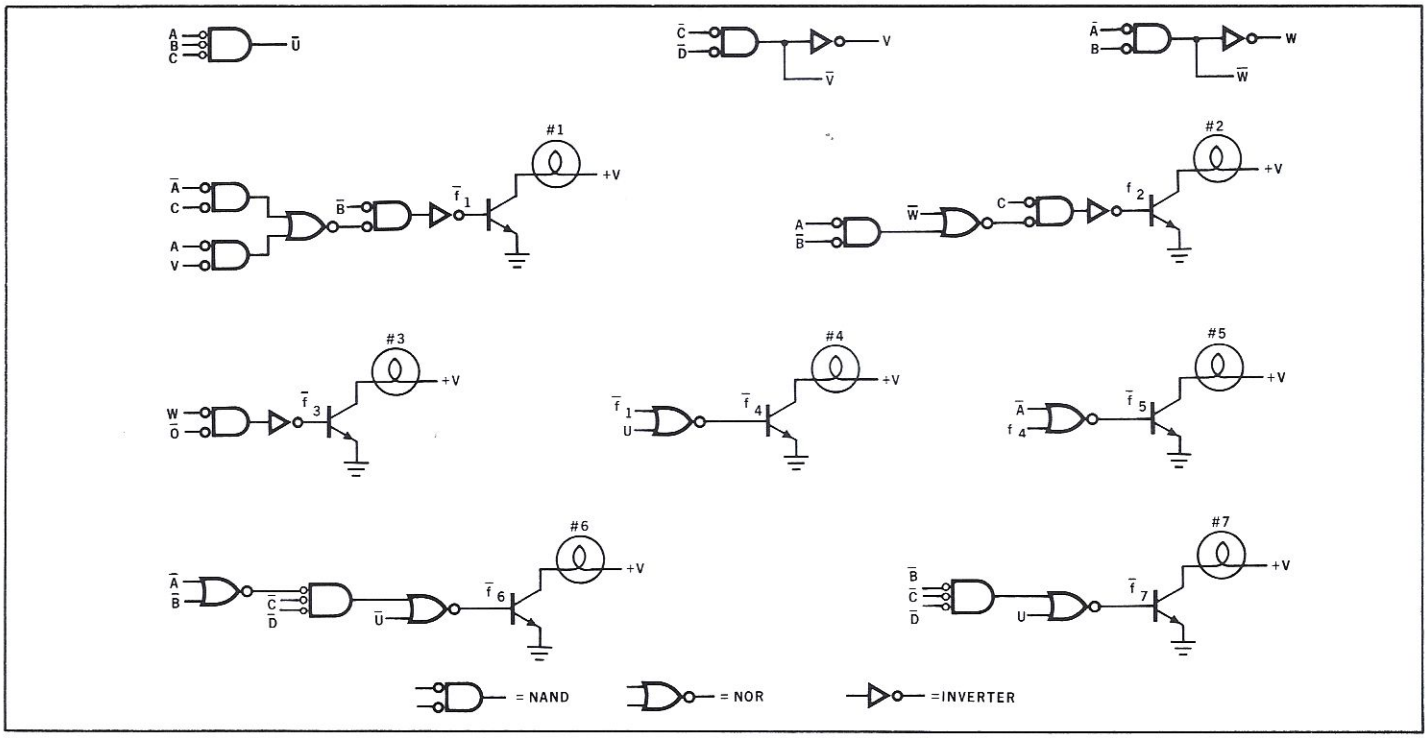


Fig. 6. Decoding circuits for the units' seconds.

as "don't cares" in our logic. The Boolean equations governing the decoding are:

$$\overline{f}_1 = \overline{B}(A\cdot\overline{C}\cdot\overline{D} + \overline{A}\cdot C),$$
$$\overline{f}_2 = C(A\cdot\overline{B} + \overline{A}\cdot B),$$
$$\overline{f}_3 = (\overline{A}\cdot B\cdot\overline{C}),$$
$$\overline{f}_4 = \overline{B}(A\cdot\overline{C}\cdot\overline{D} + \overline{A}\cdot C) + A\cdot B\cdot C,$$
$$\overline{f}_5 = A + f_4,$$
$$\overline{f}_6 = \overline{C}\cdot\overline{D}(A + B) + A\cdot B\cdot C,$$
$$\overline{f}_7 = (\overline{B}\cdot\overline{C}\cdot\overline{D} + A\cdot B\cdot C).$$

These reduced equations can be implemented as shown in Fig. 6. Because certain logic combinations occur often, three new terms are created:

$$\overline{U} = A\cdot B\cdot C;\quad V = \overline{C}\cdot\overline{D};\quad \overline{W} = \overline{A}\cdot B.$$

Tens' Display Requires a Modulo-6 Counter

The tens' counters have to display only the numerals 0 through 5, so that the question of whether the 6 and 9 should have "bars" does not apply.

Figure 4b shows that the binary progression of the counter is actually: 0 - 1 - 3 - 7 - 6 - 4. Since it does not matter to the displays what the input to the decoder is, these values can represent the numbers 0 - 1 - 2 - 3 - 4 - 5, respectively. Only three variables are involved and thus eight distinct states are possible. Of these, the states 2 and 5 never occur, so they may appear as "don't cares" in our prime implicants. The functions governing the seven segments are as follows:

$$\overline{f}_1 = (1+2+5+6),\qquad \overline{f}_5 = (1+2+4+5+6+7),$$
$$\overline{f}_2 = (2+5+6),\qquad \overline{f}_6 = (1+2+3+5+7),$$
$$\overline{f}_3 = (2+3+5),\qquad \overline{f}_7 = (0+1+2+5).$$
$$\overline{f}_4 = \overline{f}_{1'}$$

When algebraically reduced, the equations become:

$$\overline{f}_1 = \overline{X}\cdot Y + X\cdot\overline{Y},\qquad \overline{f}_5 = \overline{Z} + X\cdot\overline{Y},$$
$$\overline{f}_2 = \overline{Y}\cdot Z,\qquad \overline{f}_6 = X,$$
$$\overline{f}_3 = Y\cdot\overline{Z},\qquad \overline{f}_7 = \overline{Y}\cdot\overline{Z}.$$
$$\overline{f}_4 = \overline{f}_{1'}$$

Implementing these equations yields the logic configuration in Fig. 7.

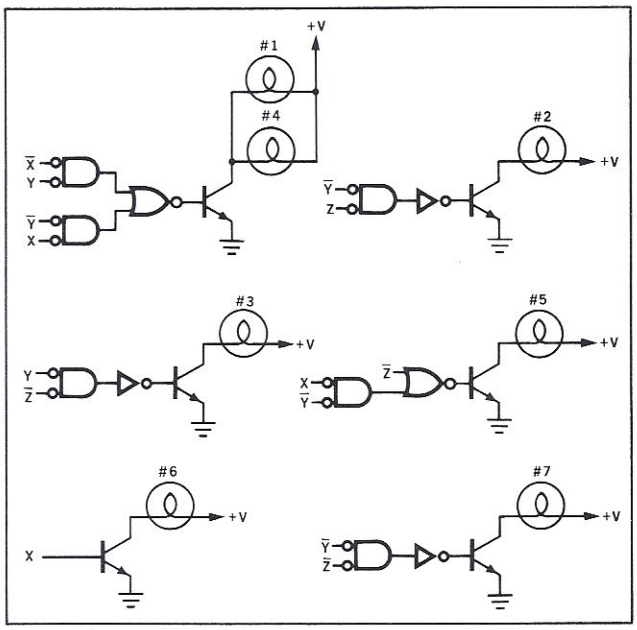


Fig. 7. Decoding circuits for the tens' seconds.

The hours' tens' circuit is a completely different circuit from the other tens' counters. Since a new cycle starts on the count of 12:59:59 + 1 second, a single flip-flop may be used. The hours' tens' flip-flop is turned ON at 9:59:59 + 1 second and remains ON until the new cycle is started. During this time, segments 2 and 3 of the hours' tens' indicator are illuminated. At all other times this indicator is extinguished.